SPI-C2160-LLVA
SPI-Q7700-LLVA

Single Host Board

User's Manual

Version 1.0

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Appendix A

Appendix B

How to Use This Manual

The manual describes how to configure your SPI-C2160-LLVA series system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Host Board.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this series model of single host board.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and Compact Flash to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides various useful tips to quickly get SPI-C2160-LLVA series running with success. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual is subject to change without prior notice. These changes will be incorporated in new editions of the document. **CONTEC** may make supplement or change in the products described in this document at any time.

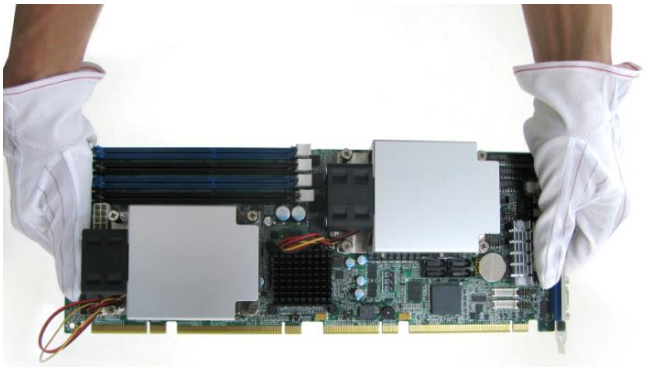
Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.contec.com/.

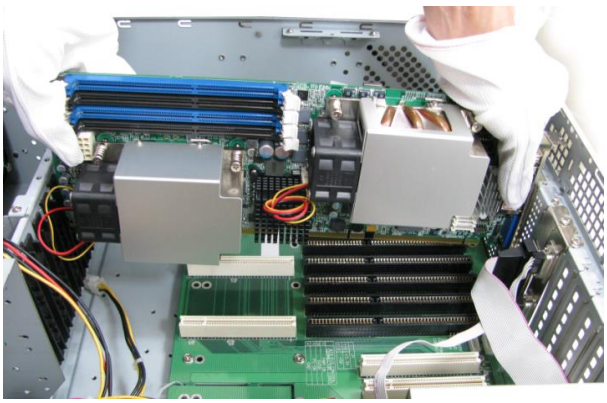
Notice
SBC Handling and Installation Notice

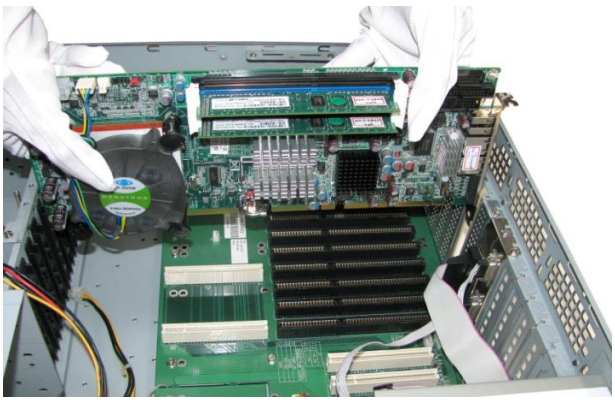
- Handling and Installing SBC

Caution: Do not just hold any single side of the SBC; hold evenly on both sides!

- Heavy processor cooler may bend the SBC when SBC being held just on one side.
- The bending may cause soldering or components damaged.







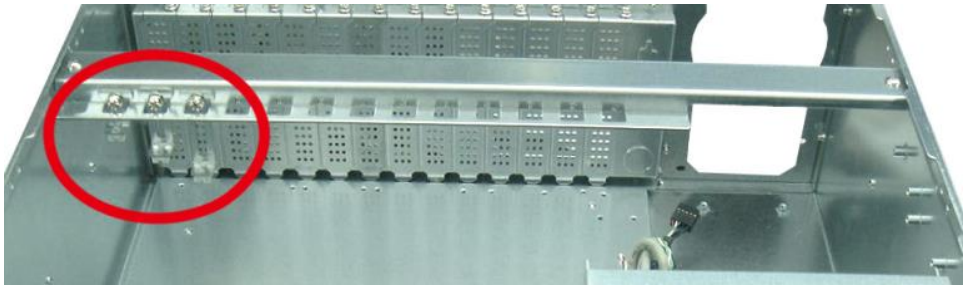
■ Fix your SBC in System

Caution: Suggest your S.I or vendor to use a metal bracket to hold/fix the desktop or server grade SBC to avoid the vibration damage during transportation. Heavy processor cooler may bend the SBC when systems are during transportation without any holder.

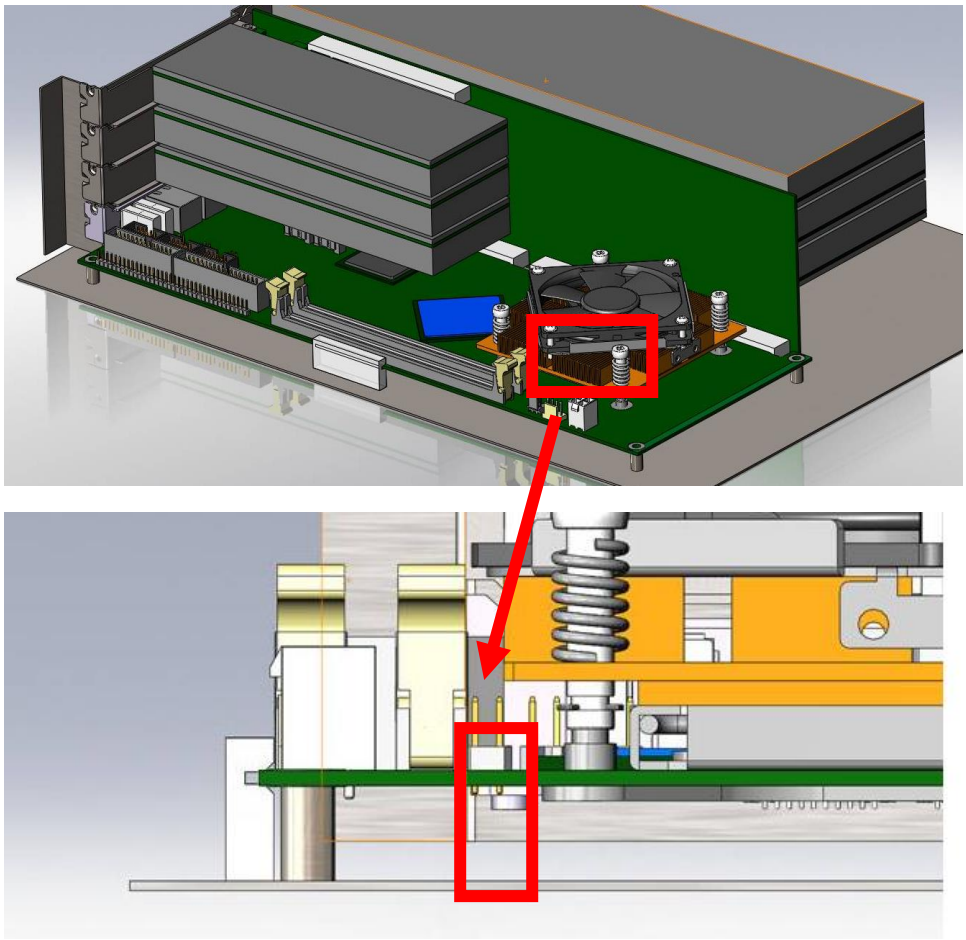
Example:

- 4U chassis :

  ➔ Use L type mental or plastic or rubber bracket to hold SBC.



- 2U or 1U chassis: a mental bracket on the bottom of chassis to balance and support SBC from bending.



Chapter 1
System Overview

1.1 Introduction

SPI-C2160-LLVA series, the PICMG 1.3 SHB (Single Host Board) supports the Intel® Core i3/i5/i7 and Xeon E3-1200v2 series processors. The attractive Core i3/i5/i7 and Xeon E3-1200v2 family processors not only posses amazing parallel computing power but also support ECC memory. That makes the system more powerful.

The SHB adopted Intel® C216 / Q77 chipset and Core i7/i5/i3/Xeon E3-1200v2 family processors. The Core i series /Xeon E3-1200v2 family processors integrated Intel® integrated graphics engine that supports 3D performance, DirectX11, Shader model 4.0, and OpenGL 3.1. More than that, user could utilize even higher-end, the latest PCI Express x16 interface graphics card via backplane.

SPI-C2160-LLVA series built with dual Intel® Gigabit Ethernet. Two DDR3 long DIMM sockets support system memory up to 16GB. Two SATA 600 ports and Four SATA 300 ports (dual ports via backplane) support RAID 0, 1, 5, 10. Support multiple display by DVI-I (DVI-D + VGA) on bracket and HDMI ports. The SBC also equipped with four USB 3.0 ports (dual ports on bracket). It can offer 5Gbps data transfer rate which is higher than the current USB 2.0.

To meet bandwidth of storage and expansion cards requirement, the SPI-C2160-LLVA series were designed flexible with four PCI Express lanes via backplane. Those four PCI Express lanes could be four PCI Express x1 links or one PCI Express x4 link by different bios support. Four PCI Express x1 links configuration can support more PCI Express x1 devices via backplane and one PCI Express x4 link configuration can support RAID card or special add-on cards such as image processing board. In addition, the flexible configuration can be leveraged with bridge on backplane to support more PCI or PCI-X slots that benefits industries with legacy support. PCI Express x16 from processors can be one PCI Express x16 or two PCI Express x8 or One PCI Express x8 + Two PCI Express x4 by jumper setting with C216 chipset. It only supports one PCI Express x16 with Q77 chipset. Intel C216 chipset be very flexible for customer to adopt with server or non-server BP.

Advanced Management Technology (AMT) 8.0 is feature that SPI-C2160-LLVA series equipped with Xeon E3-1200v2 family and Core i5/i7 processors (Core i3 doesn't support AMT). This technology provides remote access capability via Intel® Gigabit Ethernet controller. The new technology is a hardware-based solution that uses out-of-band communication for system management access to client systems. Beside that, the hardware and software information can be gathering by 3rd party software then storage in SPI interface EEPROM. Therefore, asset management could be done at the same time.

ROBO-8111G2AR series features:

- Support Intel® Xeon E3-1200v2 family/Core i3 processors on SPI-C2160-LLVA and Core i7/i5 processors on SPI-Q7700-LLVA in an LGA1155 socket
- Two 240-pin DDR3 ECC SDRAM DIMM socket, support for DDR3 1333/1066 DIMMs, up to 16GB system memory
- Intel® Xeon E3-1200v2 family and Core i7/i5/i3 processor integrated graphic engine that supports MPEG-2 Decode, DirectX 11, OpenGL 3.1 and Shader Model 4.0
- Equipped dual Intel Gigabit Ethernet ports
- Support iAMT 8.0 on some sku
- Support two SATA 600 and four SATA 300 ports (dual ports via backplane)
- Support four USB 3.0 ports (dual ports on bracket)
- One PCI Express x16 external expansion, one PCI Express x4 link (can be configured as four PCI Express x1) and four PCI devices via backplane

The PICMG 1.3 SHB is the best solution of applications such like flight simulation, image processing, Medical, factory automation and so on that need performance of display and storage.

1.2 Check List

The SPI-C2160-LLVA package should cover the following basic items:

- ✓ One SPI-C2160-LLVA single host board
- ✓ One dual Serial ports cable kit
- ✓ One single Parallel port cable kit
- ✓ One FDD cable
- ✓ One 7-pin SATA 300 signal cable
- ✓ One SATA 600 signal cable
- ✓ One Installation Resources CD-Title

Optional: One bracket with PS/2 keyboard and mouse

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**

- Intel® Xeon E3-1200v2 family and Core i3 Processor on SPI-C2160-LLVA
- Intel® Core i7/i5 Processor on SPI-Q7700-LLVA

- **BIOS**

- Phoenix system BIOS with SPI Serial CMOS EEPROM with easy upgrade function ACPI, DMI, Green function and Plug and Play Compatible

- **Main Memory**

- Support dual-channel DDR3 memory interface
- ECC, non-buffered DIMMs only on SPI-C2160-LLVA
- non-ECC, non-buffered DIMMs only on SPI-Q7700-LLVA
- -Two DIMM sockets support 1333/1600 DDR3-SDRAM up to 16GB System Memory

- **L2 Cache Memory**

- Built-in Processor

- **Chipset**

- Intel® C216 /Q77 chipset

- **Bus Interface**

- Follow PICMG 1.3 Rev 1.0 standard (PCI Express and PCI)
- Support four PCI Express x1 (can be aggregated as one PCI Express x4) through backplane by different bios
- Support four PCI devices through backplane
- Support one PCI Express x16 or two PCI Express x8 or One PCI Express x8 + Two PCI Express x4 by jumper setting on SPI-C2160-LLVA
- Only support one PCI Express x16 on SPI-Q7700-LLVA

- **SATA**

- Four SATA 300 ports on-board (dual ports via backplane) and two SATA 600 ports

- **Floppy Drive Interface**

- Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD

- **Serial Ports**

- Support one RS232 and one RS232/422/485 selectable ports

- **Parallel Port**

- Support one parallel port with SPP, EPP and ECP modes

- **USB Interface**
- Support ten USB 2.0 (Universal Serial Bus) ports (six USB ports on-board and four USB ports via backplane)
- Support four USB 3.0 ports (dual ports on bracket that dedicated to keyboard & mouse; two ports on board for high-speed I/O peripheral devices)

- **PS/2 Mouse and Keyboard Interface**
- Support one 10-pin header for external PS/2 keyboard/mouse connection

- **Auxiliary I/O Interfaces**
- System reset switch, external speaker, Keyboard lock and HDD active LED, etc

- **Real Time Clock/Calendar (RTC)**
- Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention

- **Watchdog Timer**
- Support WDT function through software programming for enable/disable and interval setting
- Generate system reset

- **On-board VGA**
- Processors integrated graphics, share system memory up to 1GB for system with greater than or equal to 192MB of system memory

- **On-board Ethernet LAN**
- Dual Intel® PCI Express x1 interface based Gigabit Ethernet to support RJ-45 connector
- Built with Intel 82579LM and 82574L Ethernet controller

- **High Driving GPIO**
- Support 8 programmable high driving GPIO

- **Cooling Fans**
- Support one 4-pin power connector for CPU fan and one 3-pin power connector for system fan

- **System Monitoring Feature**
- Monitor CPU temperature, system temperature and major power sources, etc.

- **Bracket**
- Support dual Ethernet port with 2 indicators, dual USB ports and one DVI-I port

- **Outline Dimension (L X W)**
- 338.5mm (13.33") X 126.39mm (4.98")

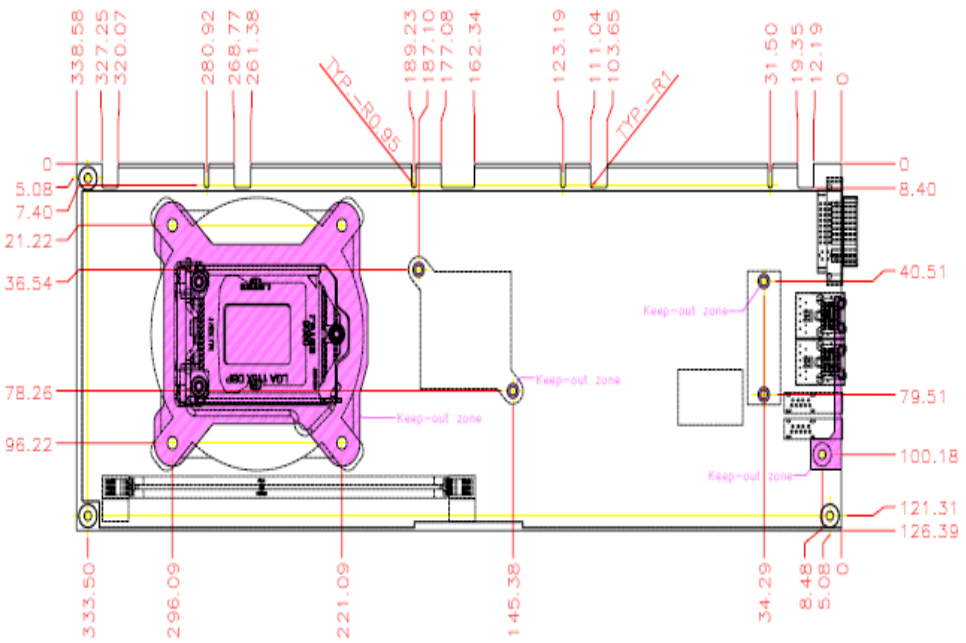
- **Power Requirements**
- +12V (CPU)@ 1.12A
- +12V (System)@ 2.64A
- +5V @ 2.22A
- Test Programs: BurnIn Test V6.0
- Run Time: Full loading 30 Min.
- Test configuration:

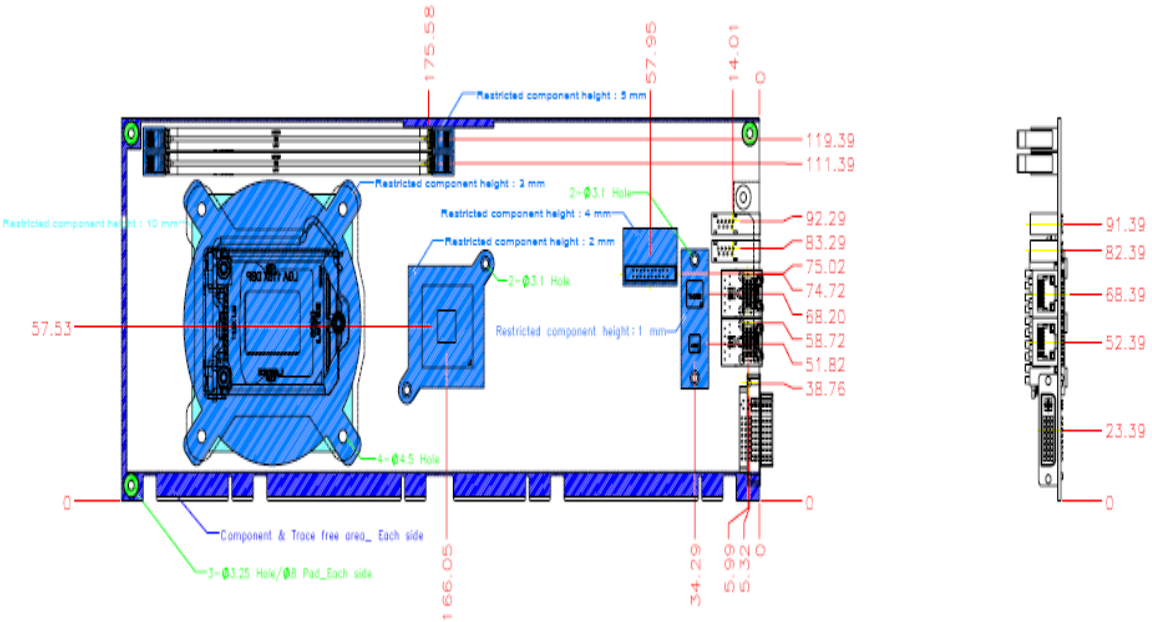
1.4 System Configuration

	System Configuration
CPU Type	Genuine Intel® CPU 2.20Hz L3:8M
SBC BIOS	CONTEC, Inc. ROBO-8111 BIOS Rev:R1.00.W0
Memory	Transcend DDR3 1333 1GB*1 (SEC K4B1G0846F)
VGA Card	Onboard Intel® Ivy Bridge HD Graphics
VGA Driver	Onboard Intel® Ivy Bridge HD Graphics Version 8.15.10.2568
LAN Card	Onboard Intel® 82574L/82579LM Gigabit Network Connection Controller
LAN Driver	Intel® 82574L/82579LM Gigabit Network Connection Version 11.11.43.0/11.14.32.0
Audio Card	Onboard Realtek ALC662 High Definition Audio Controller
Audio Driver	Realtek ALC662 High Definition Audio Version 6.0.1.6482
CHIP Driver	Intel® Chipset Device Software Version 9.3.0.1016
SATA HDD	WD WD6402AAEX 640GB
SATA CDROM	ASUS DRW-24B3ST DVD-ROM
Power Supply	FSP400-60PFN
Backplane	PBPE-06P2 R0

- Operating Temperature:
- 0°C ~ 55°C (23°F ~ 140°F)
- Storage Temperature
- -20°C ~ 80°C
- Relative Humidity
- 5% ~ 90%, non-condensing

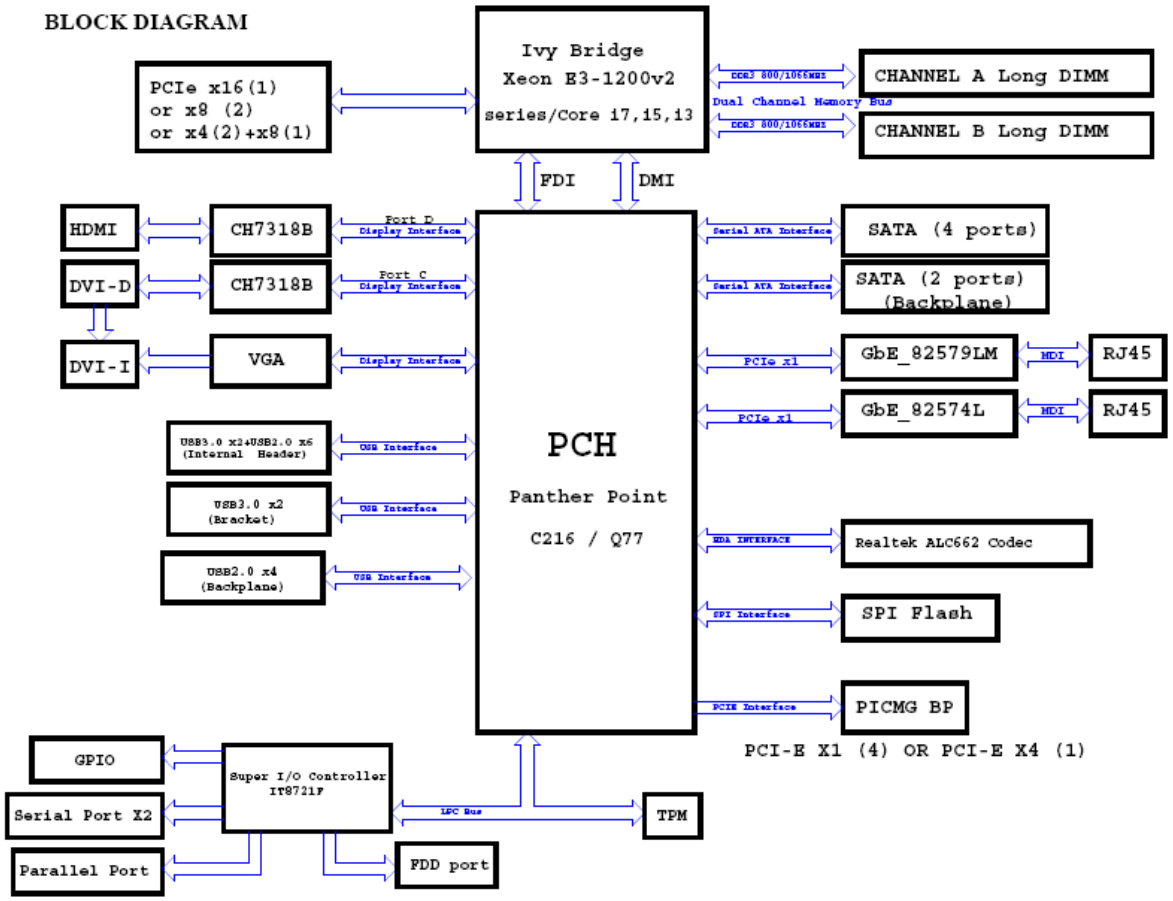
1.4.1 Mechanical Drawing





1.5 System Architecture

All of details operating relations are shown in SPI-C2160-LLVA series System Block Diagram.



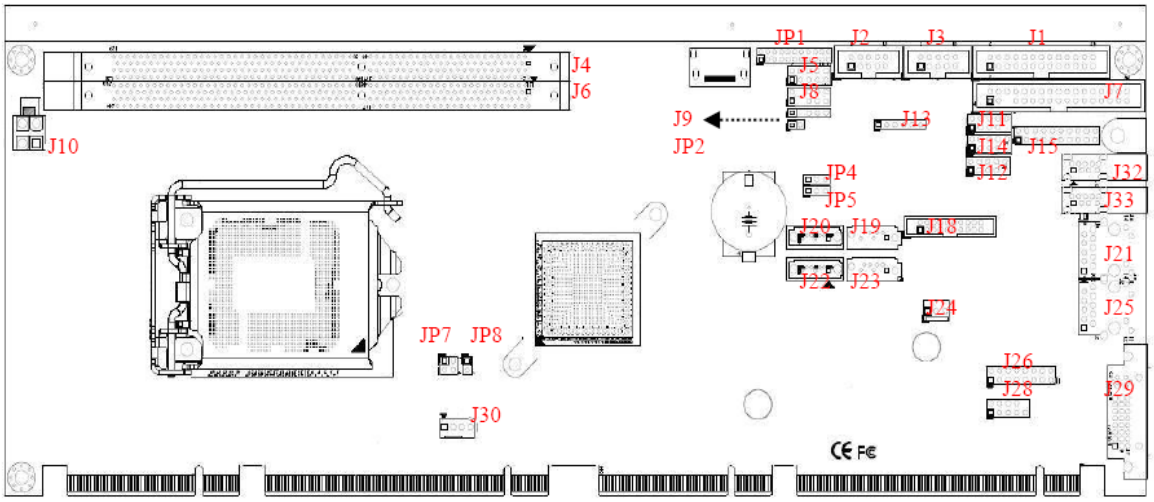
SPI-C2160-LLVA series System Block Diagram

Chapter 2
Hardware Configuration

This chapter gives the definitions and shows the positions of jumpers, headers and connectors. All of the configuration jumpers on SPI-C2160-LLVA series are in the proper position. The default settings shipped from factory are marked with an asterisk ( ).

2.1 Jumper Setting

In general, jumpers on the single board computer are used to select options for certain features. Some of the jumpers are designed to be user-configurable, allowing for system enhancement. The others are for testing purpose only and should not be altered. To select any option, cover the jumper cap over (SHORT) or remove (NC) it from the jumper pins according to the following instructions. Here NC stands for "Not Connect".



Jump Setting List

★is mean default

JP1: COM2 Function Selection

JP1	Signal Description
5-6, 9-11, 10-12, 15-17, 16-18 Short	RS-232 ★
3-4, 7-9, 8-10, 13-15, 14-16, 21-22 Short	RS-422
1-2, 7-9, 8-10, 19-20 Short	RS-485

JP2:AUTO Power Button Select

JP2	Signal Description
Short	Auto power button enable
Open	Auto power button disable ★

JP3:WDT Function Select(Reserved)

JP3	Signal Description
Short	enable
Open	disable ★

JP4:Config/Recovery Select

JP4	Signal Description
1-2 Short	Normal ★
2-3 Short	No Reboot Configure
OPEN	Recovery

JP5: CMOS Clear

JP5	Signal Description
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents

JP6: Second CMOS Clear (Reserved)

JP6	Signal Description
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents

JP7: PCI Express Bifurcation Selection

JP7	Signal Description
Short (1-2 , 3-4)	1 x8, 2 x4 PCI Express (Support Three slot)
Short (1-2),Open(3-4)	2 x8 PCI Express (Support Two slot)
Open (1-2 , 3-4)	1 x16 PCI Express (Support One slot) ★
Open (1-2),Short (3-4)	Reserved

JP8: VCCSA Voltage Selection

JP8	Signal Description
1-2 Short	0.85 V ★
1-2 Open	0.925V

JP9: Debug/Program Debug Only

JP9	Signal Description
1	GND
2	SMBUS DATA
3	SMBUS CLK

JP10: Debug/Program Only

JP10	Signal Description
1	GND
2	VPGM
3	GND

JP11: SPI Device Selection

JP11	Signal Description
1-2 Short , 3-4 Open	Device 0 ★
1-2 Open 3-4 Short	Device 1

JP12: ME Function Disable (for debug)

JP12	Signal Description
1-2 Short	ME function disable
1-2 Open	ME function enable ★

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
J1	Parallel Port Connector	
J2	Serial Port 1 Connector	
J3	Serial Port 2 Connector	
J4/J6	DDR3 Slot	
J5	GPIO header	
J7	Floppy Connector	
J8	PS/2 Keyboard/Mouse Header	
J9	SMBUS header	
J10	+12V Power Connector	
J11/J12/J14	USB Header	
J13	CIR Header	Reserved
J15	USB3.0 header	
J19/J20/J22/J23	SATA Connector	
J21	RJ-45 Connector 82574L	
J24	FAN 1 (SYSTEN FAN) Power Connector	
J25	RJ-45 Connector 82579LM	
J26	Front Panel Pin HDR	
J28	Audio Connector	
J29	DVI Connector	
J30	FAN 2 (CPU FAN) Power Connector	
J32/J33	USB3.0 Connector	

J1 Parallel Port Connector

PIN No.	Signal Description	PIN No	Signal Description
1	Strobe#	2	Auto Form Feed#
3	Data0	4	Error#
5	Data1	6	Initialization#
7	Data2	8	Printer Select IN#
9	Data3	10	Ground
11	Data4	12	Ground
13	Data5	14	Ground
15	Data6	16	Ground
17	Data7	18	Ground
19	Acknowledge#	20	Ground
21	Busy	22	Ground
23	Paper Empty	24	Ground

PIN No.	Signal Description	PIN No	Signal Description
25	Printer Select	26	NC

J2: COM1 Serial Port

PIN No.	Signal Description
1	DCD
2	DSR
3	RXD
4	RTS
5	TXD
6	CTS
7	DTR
8	RI
9	Ground
10	N/C

J3 : Serial Port 2 Connector

PIN No.	Signal Description	PIN No	Signal Description
	RS-232	RS-422	RS-485
1	DCD (Data Carrier Detect)	TX-	DATA-
2	DSR (Data Set Ready)	N/C	N/C
3	RXD (Receive Data)	TX+	DATA+
4	RTS (Request to Send)	N/C	N/C
5	TXD (Transmit Data)	RX+	N/C
6	CTS (Clear to Send)	N/C	N/C
7	DTR (Data Terminal Ready)	RX-	N/C
8	RI (Ring Indicator)	N/C	N/C
9	GND (Ground)	GND	GND
10	N/C	N/C	N/C

J5: GPIO Header

PIN No.	Signal Description	PIN No	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

J7:Floppy Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select
3	Ground	4	N/C
5	N/C	6	N/C
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	N/C
13	Ground	14	Drive Select A#
15	Ground	16	N/C
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	N/C	30	Read Data#
31	Ground	32	Head Select#
33	N/C	34	Disk Change#

J8: PS/2 Keyboard/Mouse Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	N/C	4	N/C
5	Ground	6	Ground
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Keyboard Clock

J9:SMBUS Header

PIN No.	Signal Description
1	SMBus_CLK
2	N/C
3	Ground
4	SMBus_DAT
5	+5V

J11/J12/J14/: USB Header

PIN No.	Signal Description	PIN No.	Signal Description
1	5V Dual	2	5V Dual
3	USB-	4	USB-
5	USB+	6	USB+
7	Ground	8	Ground

	Key	10	N/C

J13:CIR Header

PIN No	Signal Description
1	+5V
2	N/C
3	CIRRX
4	Ground
5	CIRTX
6	N/C

J5: USB3.0 Header

PIN No.	Signal Description	PIN No.	Signal Description
1	+5V	2	KEY
3	USB3_RX-	4	+5V
5	USB3_RX+	6	USB3_RX-
7	GND	8	USB3_RX+
9	USB3_TX-	10	GND
11	USB3_TX+	12	USB3_TX-
13	GND	14	USB3_TX+
15	USB2_D-	16	GND
17	USB2_D+	18	USB2_D-
19	NC	20	USB D+

J24: System Fan Connector

PIN No.	Signal Description
1	Ground
2	FAN PWM_CONTROL
3	Sense output

J26:Front Panel Pin HDR

PIN No	Signal Description	PIN No	Signal Description
1	PWR_LED(+)	2	Speaker(+)
3	PWR_LED(-)	4	N/C
5	J25 LAN1_ACT(+)	6	N/C
7	J25 LAN1_LINK(-)	8	Speaker(-)
9	J21 LAN2_LINK(-)	10	NC
11	J21 LAN2_ACT(+)	12	NC
13	HDD_LED(+)	14	NC
15	HDD_LED(-)	16	NC

J28: Audio MIC/Line-in/Line-out Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	MIC with Reference Voltage	2	Analog Ground
3	Line-in Left Channel	4	Analog Ground
5	Line-in Right Channel	6	Analog Ground
7	Line-out Left Channel	8	Analog Ground
9	Line-out Right Channel	10	N/C

J30: CPU Fan Connector

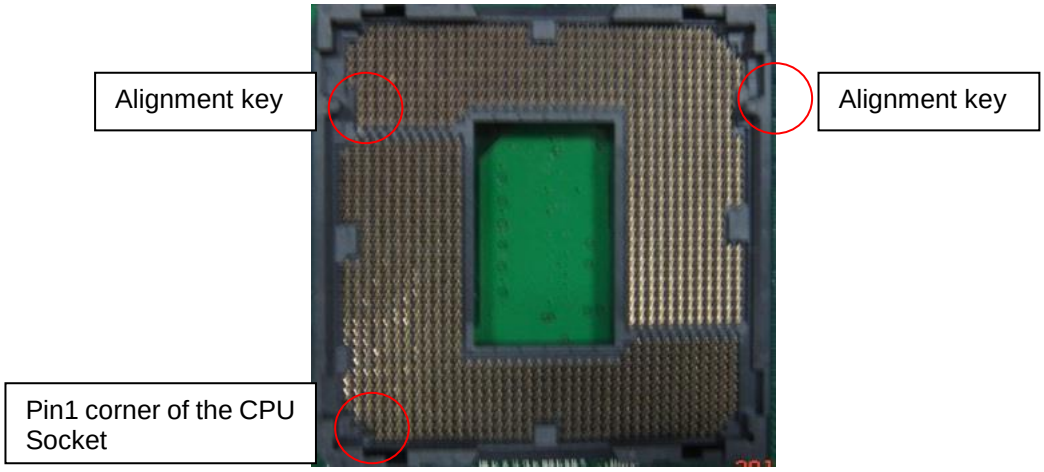
PIN No.	Signal Description
1	Ground
2	+12V
3	Sense output
4	FAN PWM_CONTROL

Chapter 3
System Installation

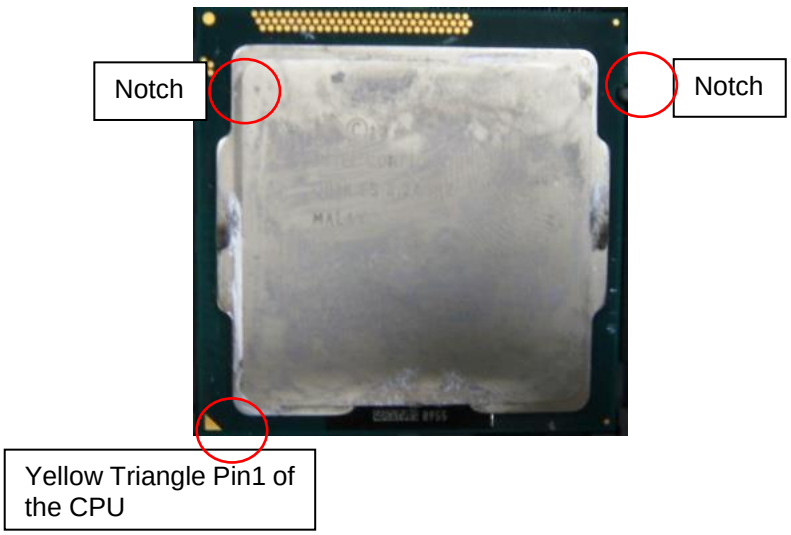
This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel LGA-1155 Processor

LGA-1155 CPU Socket



LGA-1155 CPU



Please remember to locate the alignment keys on the CPU socket of the motherboard and the notches on the CPU.

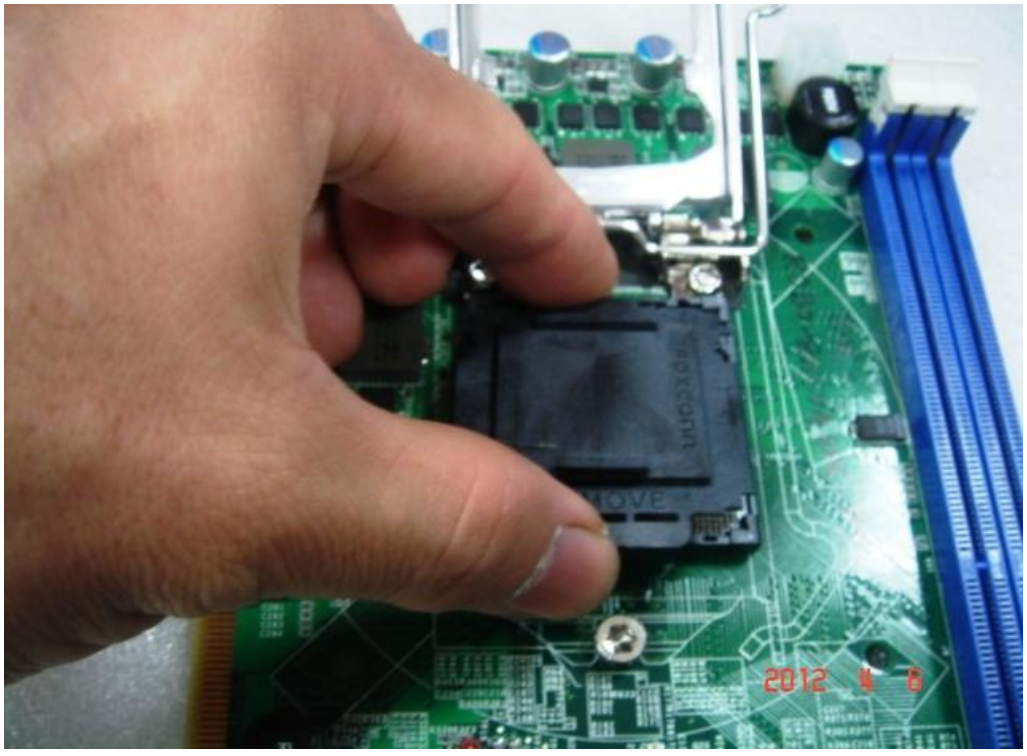
LGA-1155 CPU Installation Steps

Before install the CPU, please make sure to turn off the power first!!

1. Open the load lever.

2. Lift the load lever up to fully open.

2. Remove the plastic cap on the CPU socket. Before you install the CPU, always cover it to protect the socket pin.



4. After confirming the CPU direction for correct mating, put down the CPU in the socket housing frame. Note that alignment keys are matched.

5. Make sure the CPU has been seated well into the socket. If not, take out the CPU and reinstall.

6. Engage the load lever while pressing down lightly onto the load plate.

7. Push the CPU socket lever back into its locked position.

8. Please make sure four hooks are in proper position before you install the cooler.

3.2 Main Memory

SPI-C2160-LLVA provide 2 x240 pin DIMM sockets (Dual Channel) which supports Dual channel 1066/1333 DDR3-SDRAM as main memory, Non-ECC (Error Checking and Correcting), non-register functions. The maximum memory can be up to 16GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.

Before locking, make sure that all modules have been fully inserted into the card slots.

Note:

To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your SPI-C2160-LLVA into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position
Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place SPI-C2160-LLVA into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING
Please ensure that SBC is properly inserted and fixed by mechanism.

Note:
Please refer to section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

SPI-C2160-LLVA uses Intel Cougar Point Desktop B65 chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in SPI-C2160-LLVA CD-title.

3.3.2 Intel® Integrated Graphics Controller

SPI-C2160-LLVA uses Intel® PCH integrated graphic chipset to gain an outstanding graphic performance. SPI-C2160-LLVA supports DVI-D, HDMI dual display. This combination makes SPI-C2160-LLVA an excellent piece of multimedia hardware.

Drivers Support

Please find the Graphic drivers in the SPI-C2160-LLVA CD-title. Drivers support, Windows XP/Win7.

3.3.3 On-board Gigabit Ethernet Controllers

Drivers Support

Please find Intel 82579LM and 82574L LAN drivers in /Ethernet directory of SPI-C2160-LLVA CD-title. The drivers support Windows XP/Win7.

3.3.4 Audio Controller

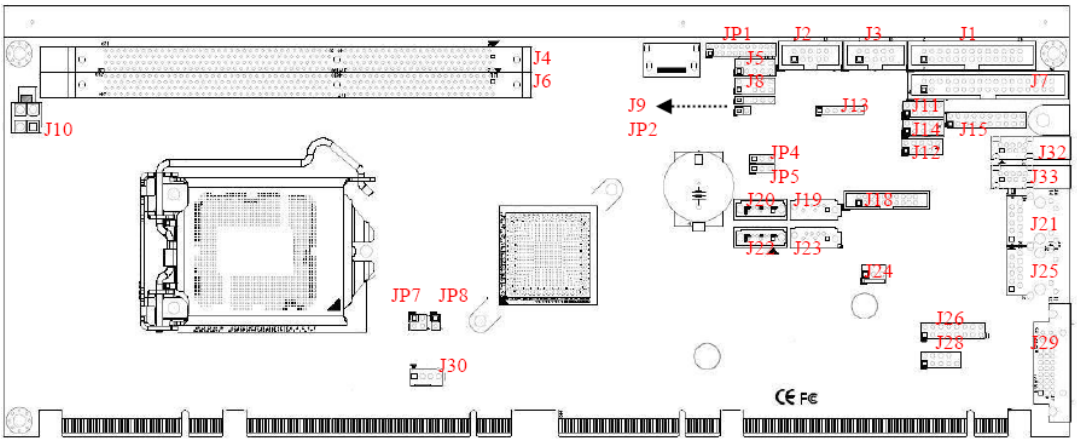
Please find Realtek ALC662-GR (High Definition Audio driver) form SPI-C2160-LLVA CD-title. The drivers support Windows XP/Win7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP5: CLEAR CMOS

JP5	Function
1-2 Short	Normal Operation ★
2-3 Short	Clear CMOS Contents



3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

SPI-C2160-LLVA allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process.

A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles. The related Control Registers of WDT are all included in the following sample program that is written in C language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out

Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed. Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to **IT8721F**/CX-L data sheet. There are two PNP I/O port addresses that can be used to configure WDT.

1) 0x2E:EFIR (Extended Function Index Register, for identifying CR index number)
2) 0x2F:EFDR (Extended Function Data Register, for accessing desired CR)
Below are some example codes, which demonstrate the use of WDT.

```
#include <stdio.h>
#include <conio.h>
#include <dos.h>

#define SIO_Port 0x2E
#define  SIO_Port2          0x4E
#define GPIO_LDN          0x07

void Enter_IT872x_SIO() {
        outportb(SIO_Port, 0x87);
        outportb(SIO_Port, 0x01);
        outportb(SIO_Port, 0x55);
        outportb(SIO_Port, 0x55);

}

void Set_LDN(unsigned char LDN) {
        outportb(SIO_Port, 0x07);
        outportb(SIO_Port+1, LDN);
        printf("LDN=%x\n", LDN);
}

void Set_Register(unsigned char offset, unsigned char value) {
        outportb(SIO_Port, offset);
        outportb(SIO_Port+1, value);
        printf("Write offset:%x = %x\n", offset, value);
}

int main(void) {

        printf("test string\n");
        Enter_IT872x_SIO();
        Set_LDN(GPIO_LDN);

        Set_Register(0x72, 0xC0);
        Set_Register(0x73, 0x05);
        printf("System will reset in 5 seconds\n");

        return 0;

}
```

3.6 GPIO

The SPI-C2160-LLVA provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

J5: General Purpose I/O Connector

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO0	2	GPIO4
3	GPIO1	4	GPIO5
5	GPIO2	6	GPIO6
7	GPIO3	8	GPIO7
9	Ground	10	+5V

```
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>

#define SIO_Port 0x2E
#define  SIO_Port2          0x4E
#define GPIO_LDN            0x07
#define GPIO_Base           0x0A00

//Enter SIO
void Enter_IT872x_SIO() {
        outp(SIO_Port, 0x87);
        outp(SIO_Port, 0x01);
        outp(SIO_Port, 0x55);
        outp(SIO_Port, 0x55);

}

//Select LDN
void Set_LDN(unsigned char LDN) {
        outp(SIO_Port, 0x07);
        outp(SIO_Port+1, LDN);
        //printf("LDN=%x\n", LDN);
}

//Set register offset to Value
void Set_Register(unsigned char offset, unsigned char value) {
```

```
	outp(SIO_Port, offset);
	outp(SIO_Port+1, value);
	//printf("Write offset:%x = %x\n", offset, value);
}

//Or register
void Or_Register(unsigned char offset, unsigned char value) {
	outp(SIO_Port, offset);
	outp(SIO_Port+1, inp(SIO_Port+1) | value);
	//printf("Write offset:%x = %x\n", offset, value);
}

//And register
void And_Register(unsigned char offset, unsigned char value) {
	outp(SIO_Port, offset);
	outp(SIO_Port+1, inp(SIO_Port+1) & value);
	//printf("Write offset:%x = %x\n", offset, value);
}
int main(void) {

	int result;
	printf("ROBO-8111 GPIO Test:\n");

	//pin1 =11
	//pin3 =12
	//pin5 =47
	//pin7 =50


	//pin2 =14
	//pin4 =35
	//pin6 =36
	//pin8 =37


	Enter_IT872x_SIO();
	Set_LDN(GPIO_LDN);

	//Enable GPIO
	//Or_Register(0xC0,0x46) //11,12,14
	//Or_Register(0xC2,0xE0) //35,36,37
	//Or_Register(0xC3,0x80) //47
	//Or_Register(0xC4,0x01) //50

	//Set Output
	Or_Register(0xC8,0x06);    //11,12
```

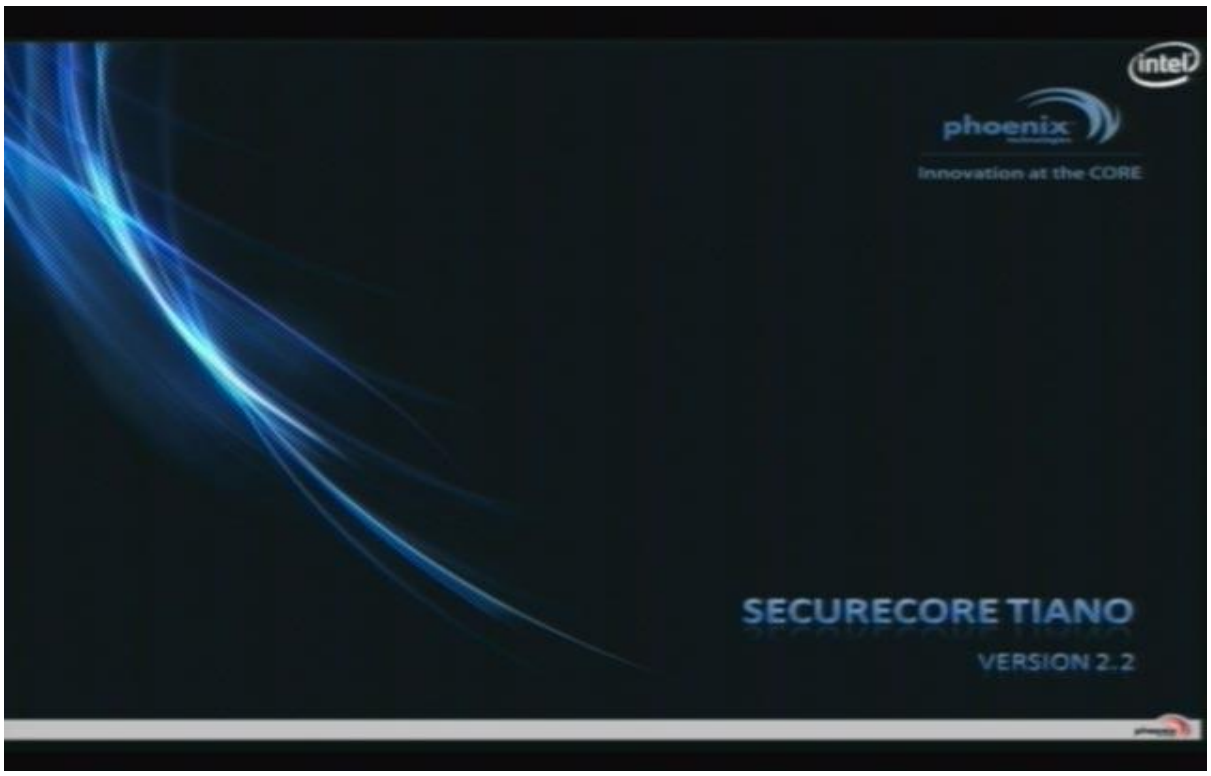
```
Or_Register(0xCB,0x80);    //47
Or_Register(0xCC,0x01);    //50

//Set Input
And_Register(0xC8,0xEF); //14
And_Register(0xCA,0x1F); //35,36,37

//output high
outp(GPIO_Base+0,0x06);  //11,12
outp(GPIO_Base+3,0x80);  //47
outp(GPIO_Base+4,0x01);  //50

result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x10) result=0;
if ((inp(GPIO_Base+2)&0xE0)!=0xE0) result=0;

if (result==0){

        printf("Test fail!!\n");

        return 1;
}


//output low
outp(GPIO_Base+0,inp(GPIO_Base+0)&0xF9);        //11,12
outp(GPIO_Base+3,inp(GPIO_Base+3)&0x7F);        //47
outp(GPIO_Base+4,inp(GPIO_Base+4)&0xFE);        //50

result=1;
if ((inp(GPIO_Base+0)&0x10)!=0x00) result=0;
if ((inp(GPIO_Base+2)&0xE0)!=0x00) result=0;

if (result==0){

        printf("Test fail!!\n");
        return 1;

}

////////////////////////////////////////////////

//Set Input
And_Register(0xC8,0xF9);  //11,12
And_Register(0xCB,0x7F); //47
And_Register(0xCC,0xFE);//50
```

```
        //Set output
        Or_Register(0xC8,0x10);     //14
        Or_Register(0xCA,0xE0);    //35,36,37

        //output high
        outp(GPIO_Base+0,0x10);  //14
        outp(GPIO_Base+2,0xE0);  //35,36,37

        result=1;
        if ((inp(GPIO_Base+0)&0x06)!=0x06) result=0; //11,12
        if ((inp(GPIO_Base+3)&0x80)!=0x80) result=0; //47
        if ((inp(GPIO_Base+4)&0x01)!=0x01) result=0; //50

        if (result==0){

                printf("Test fail!!\n");

                return 1;
        }

        //output low
        outp(GPIO_Base+0,inp(GPIO_Base+0)&0xEF);          //14
        outp(GPIO_Base+2,inp(GPIO_Base+2)&0x1F);          //35,36,37

        result=1;
        if ((inp(GPIO_Base+0)&0x06)!=0x00) result=0; //11,12
        if ((inp(GPIO_Base+3)&0x80)!=0x00) result=0; //47
        if ((inp(GPIO_Base+4)&0x01)!=0x00) result=0; //50

        if (result==0){

                printf("Test fail!!\n");
                return 1;

        }

        //getchar ();

        printf("Test Pass!!\n");
        return 1;
}
```

Chapter 4
BIOS Setup Information

SPI-C2160-LLVA uses phoenix BIOS structure stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, RUBY-PB6511 communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup - Launch System Setup



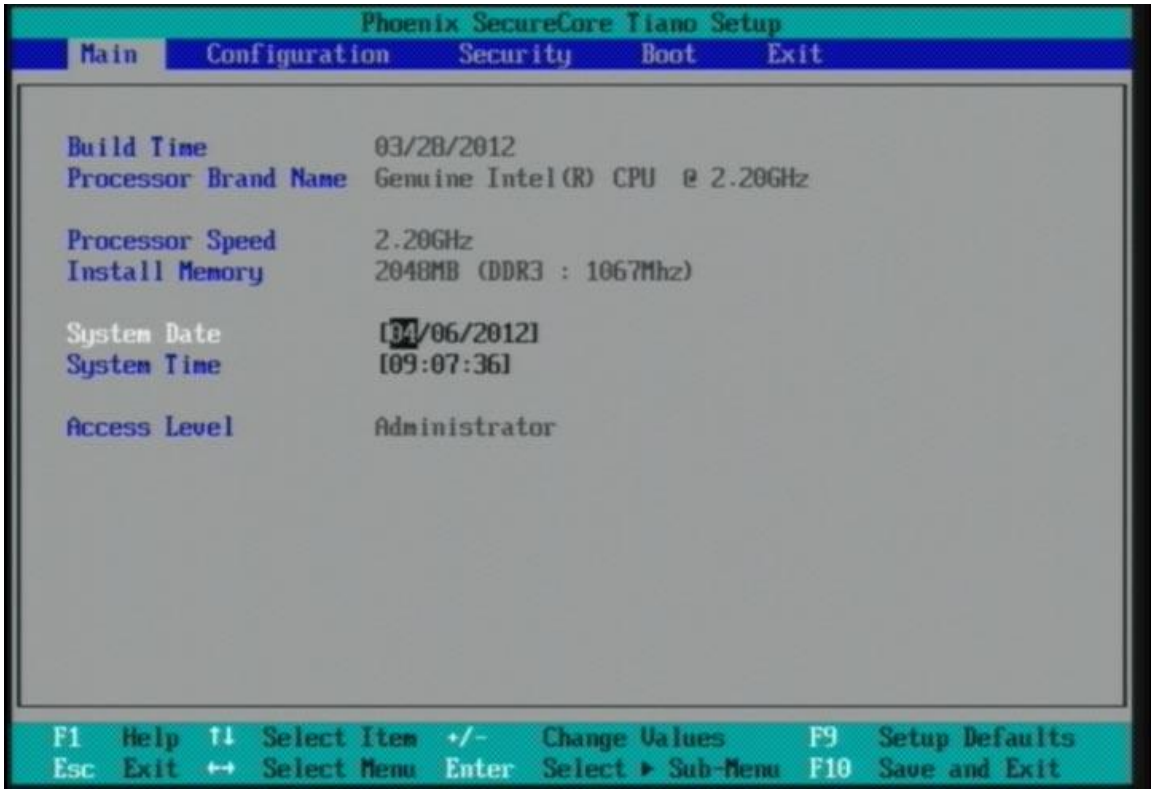
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <F2> key will enter BIOS setup screen.

Press <F2> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

4.2 Main

Use this menu for basic system configurations, such as time, date etc.



Build Time, Processor Brand Name, Processor Speed, Install Memory, etc
These items show the firmware and memory specifications of your system. Read only.

Build Time
The BIOS Release Date.

Processor Brand Name / Processor Speed
This value will change depend of different CPUs. And please make sure the Processor that you'll install will be compatible with SPI-C2160-LLVA

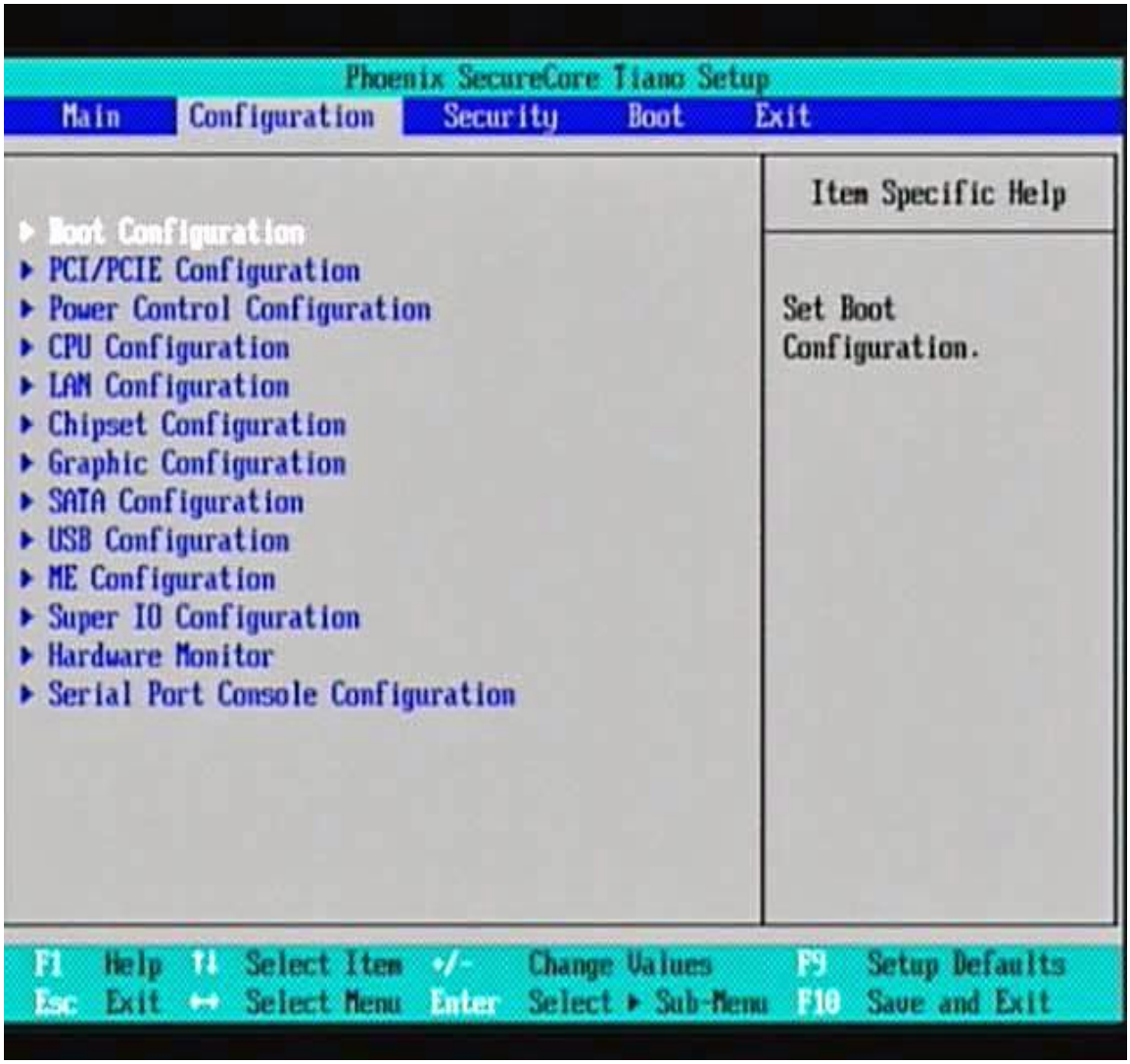
System Date
The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

System Time
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

Access Level
Read Only.

4.3 Advanced

Use this menu to set up the items of special enhanced features.

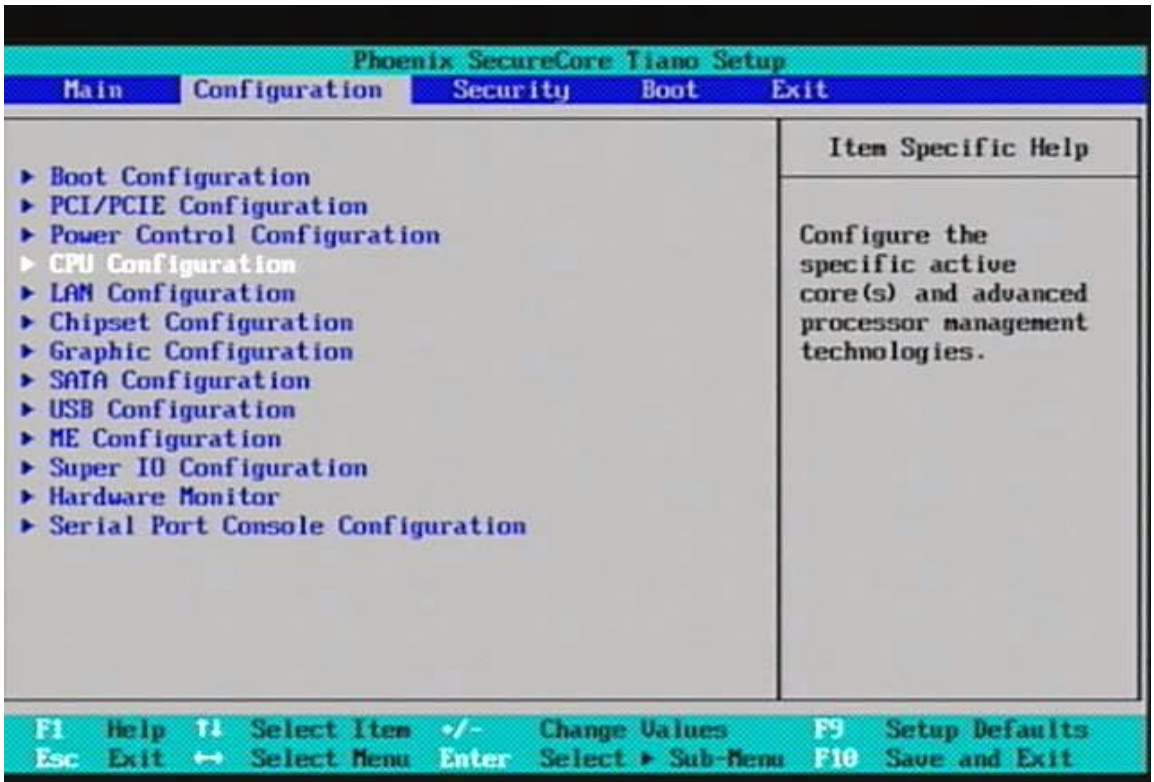


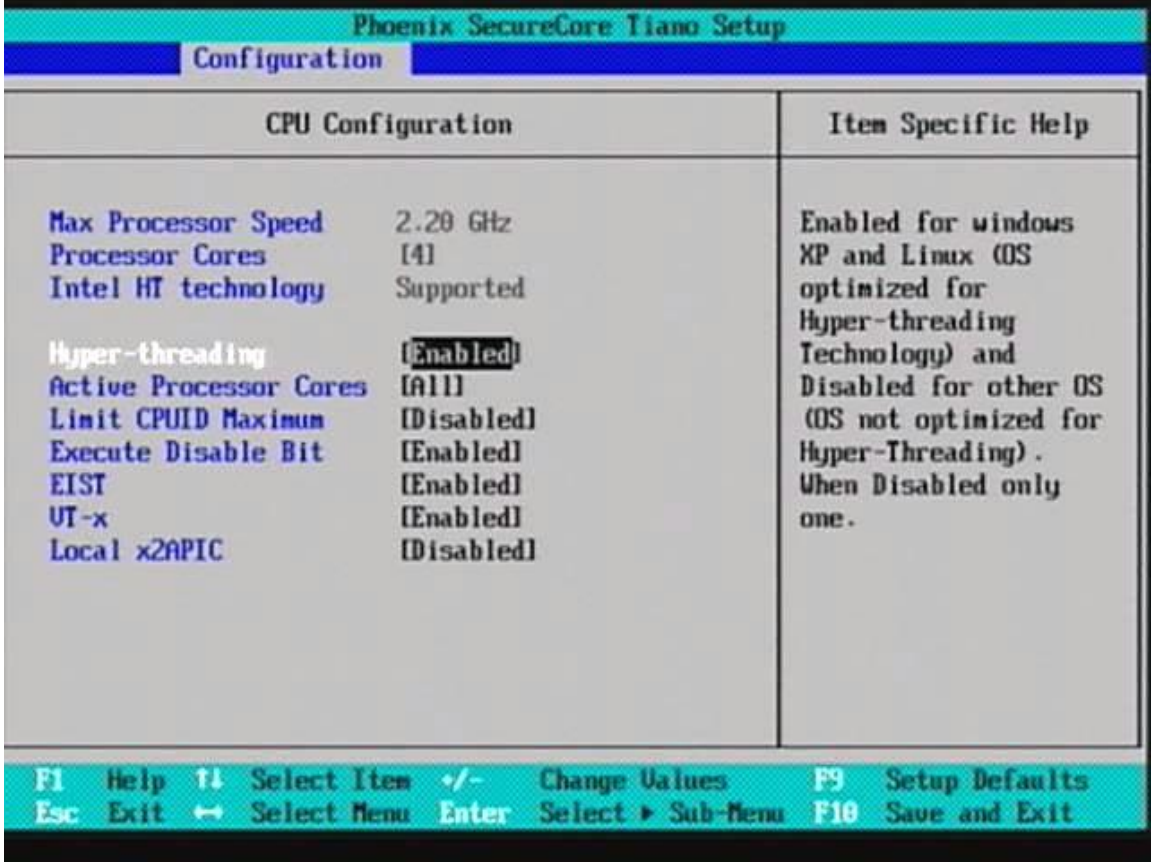
Boot Configuration
It is not necessary to make any change just take the default value.

PCI/PCIE Configuration
It is not necessary to make any change just take the default value.

Power Control Configuration

It is not necessary to make any change just take the default value.




Phoenix SecureCore Tiano Setup
Configuration
CPU Configuration
Item Specific Help
Max Processor Speed 2.20 GHz
Processor Cores [4]
Intel HT technology Supported
Hyper-threading [Enabled]
Active Processor Cores [All]
Limit CPUID Maximum [Disabled]
Execute Disable Bit [Enabled]
EIST [Enabled]
VT-x [Enabled]
Local x2APIC [Disabled]
Enabled for windows XP and Linux (OS optimized for Hyper-threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading). When Disabled only one.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit

CPU Configuration
Here you'll see the Max Processor Speed/Processor Cores/Intel HT technology then you can adjust if you want to "disabled" the Hyper-threading.

Active Processor Cores
All or select the number physical cores to enable in each processor package.

Limit CPUIP Maximum
Disabled for Windows XP.

Execute Disable Bit
Enabled Execute Disabled functionality. Also known as Data Execution revention (DEP).

EIST
Enabled

VT-x
Enabled (When enabled, a VWM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Local x2APIC
Disabled

LAN Configuration
Intel 82579LM [Enabled]
Wake on Lan [Enabled]
LAN Boot ROM [Enabled]

Chipset Configuration
VT-d [Disabled]
NB PCIe Configuration (Config NB PCI Express Setting)
Memory Configuration (Memory Configuration Parameters)

Graphic Configuration
Primary Display [Auto]
Internal Graphic [Auto]
Aperture Size [512MB]
DVMI Pre-Allocated [512MB]
DVMT Total Gfx Mem [MAX]

Primary Boot display [VBIOS Default]

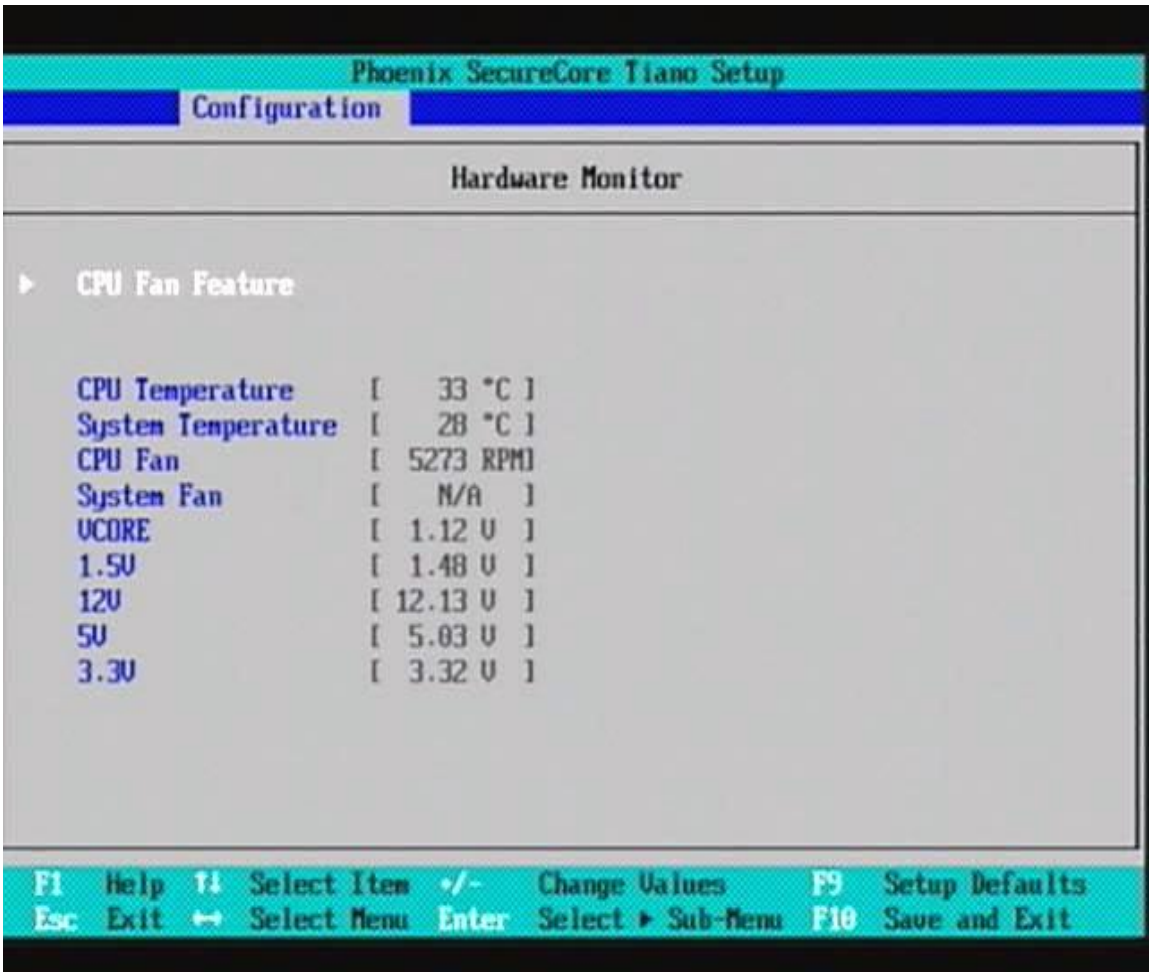
SATA Configuration
Determines how SATA controller (s) operate.

USB Configuration
Configure USB controller and other advanced setting.

ME Configuration
Configure Management Engine Technology Parameters.

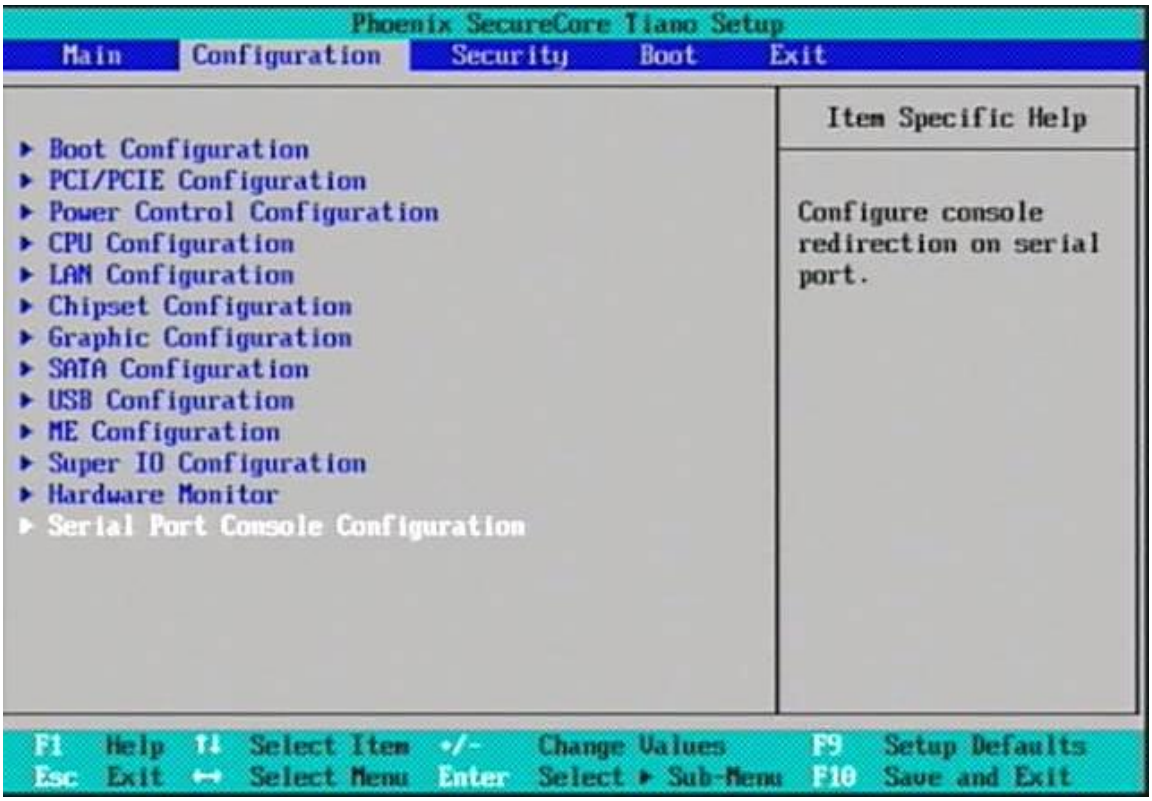
Super IO Configuration
Configure LPC Super IO

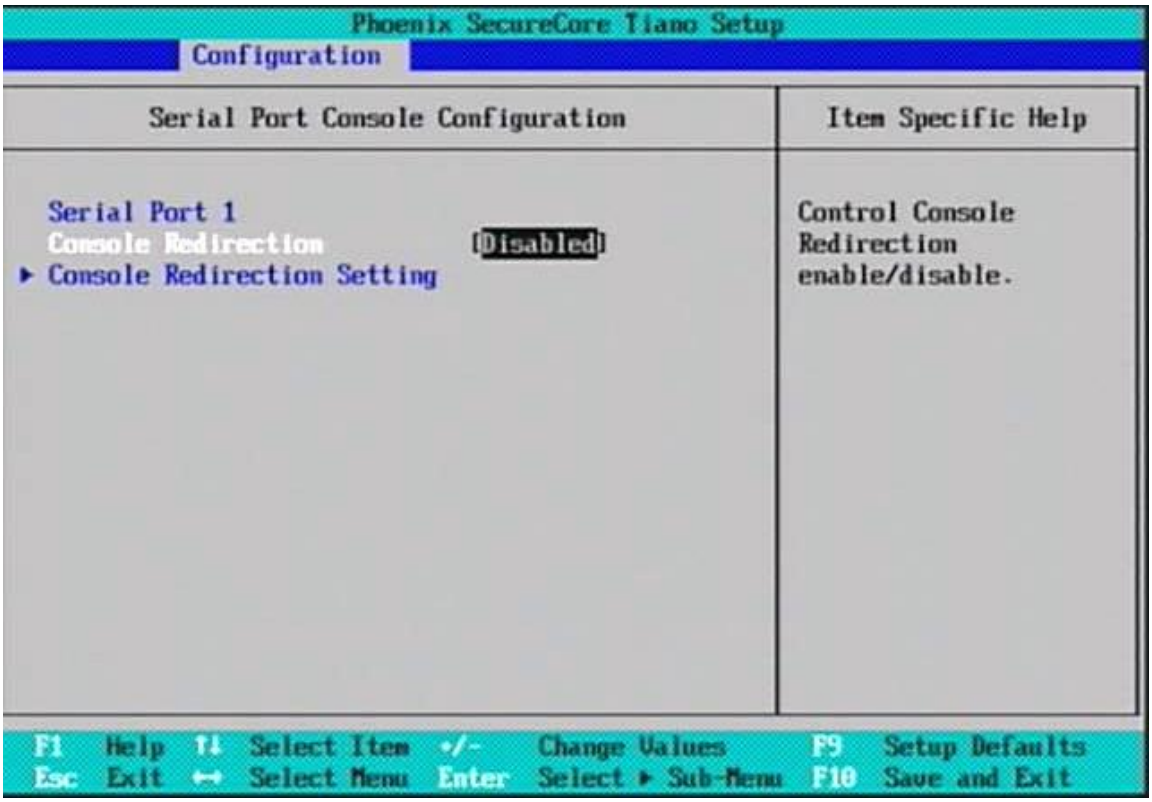
Hardware Monitor
Provide on board sensor reading information.

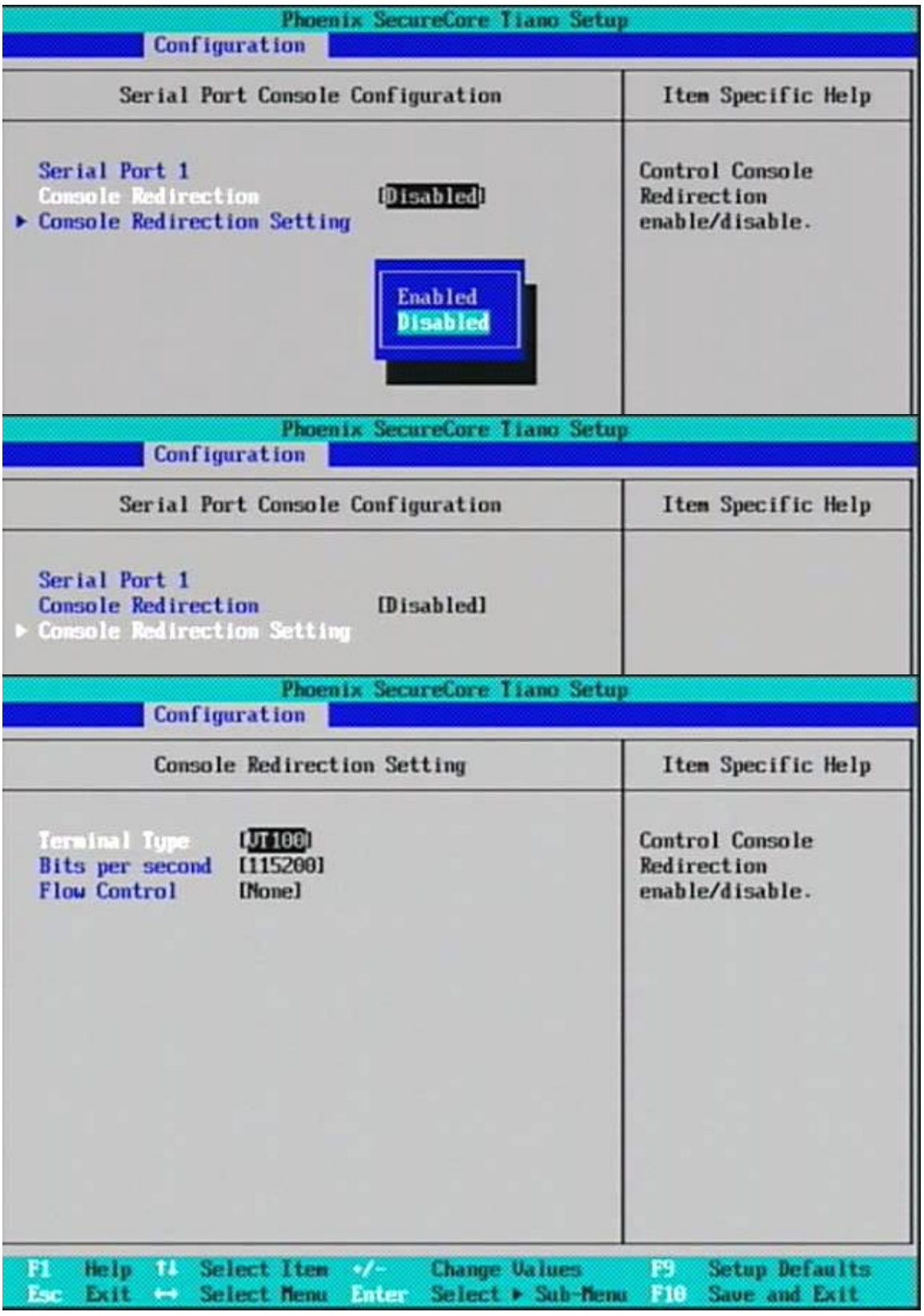

Phoenix SecureCore Tiano Setup
Configuration
Hardware Monitor
CPU Fan Feature
CPU Temperature [33 °C]
System Temperature [28 °C]
CPU Fan [5273 RPM]
System Fan [N/A]
VCORE [1.12 V]
1.5V [1.48 V]
12V [12.13 V]
5V [5.03 V]
3.3V [3.32 V]
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit

Serial Port Console Configuration

Configure console redirection on serial port.

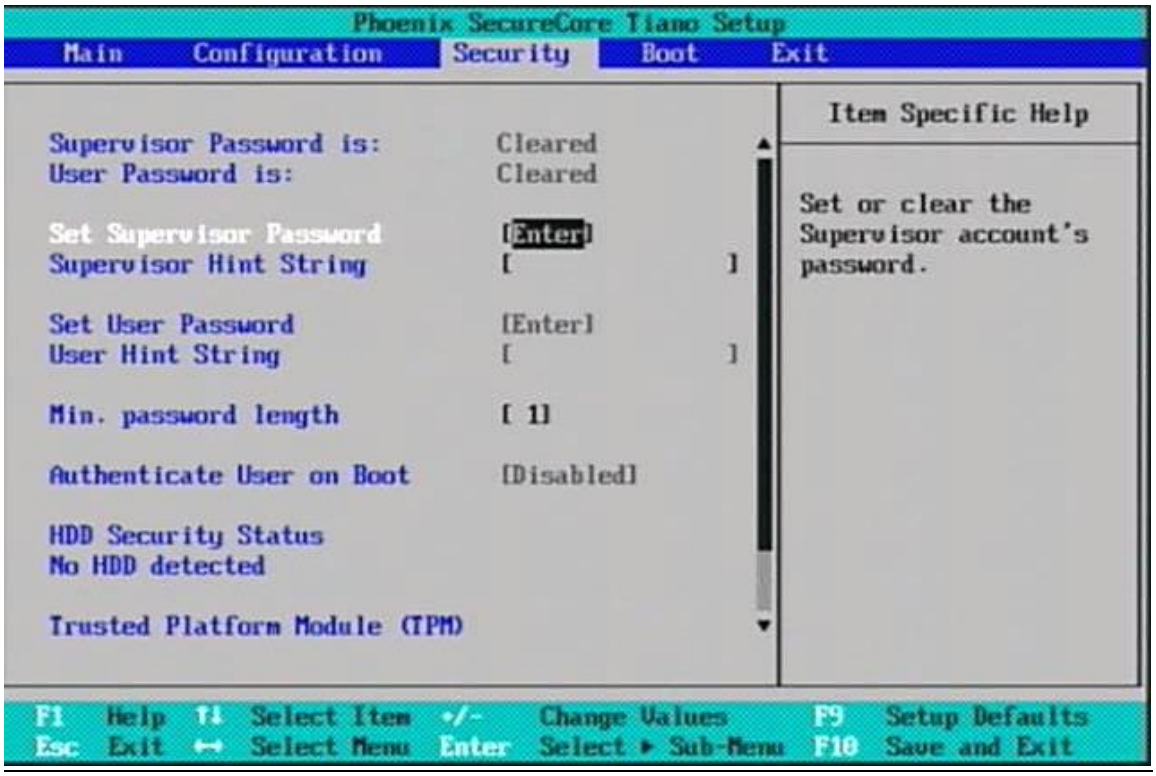



Phoenix SecureCore Tiano Setup
Configuration
Serial Port Console Configuration
Item Specific Help
Serial Port 1
Console Redirection [Disabled]
Console Redirection Setting
Control Console Redirection enable/disable.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit


Phoenix SecureCore Tiano Setup
Configuration
Serial Port Console Configuration
Item Specific Help
Serial Port 1
Console Redirection [Disabled]
▶ Console Redirection Setting
Control Console Redirection enable/disable.
Enabled
Disabled
Phoenix SecureCore Tiano Setup
Configuration
Serial Port Console Configuration
Item Specific Help
Serial Port 1
Console Redirection [Disabled]
▶ Console Redirection Setting
Phoenix SecureCore Tiano Setup
Configuration
Console Redirection Setting
Item Specific Help
Terminal Type [VT100]
Bits per second [115200]
Flow Control [None]
Control Console Redirection enable/disable.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▶ Sub-Menu F10 Save and Exit

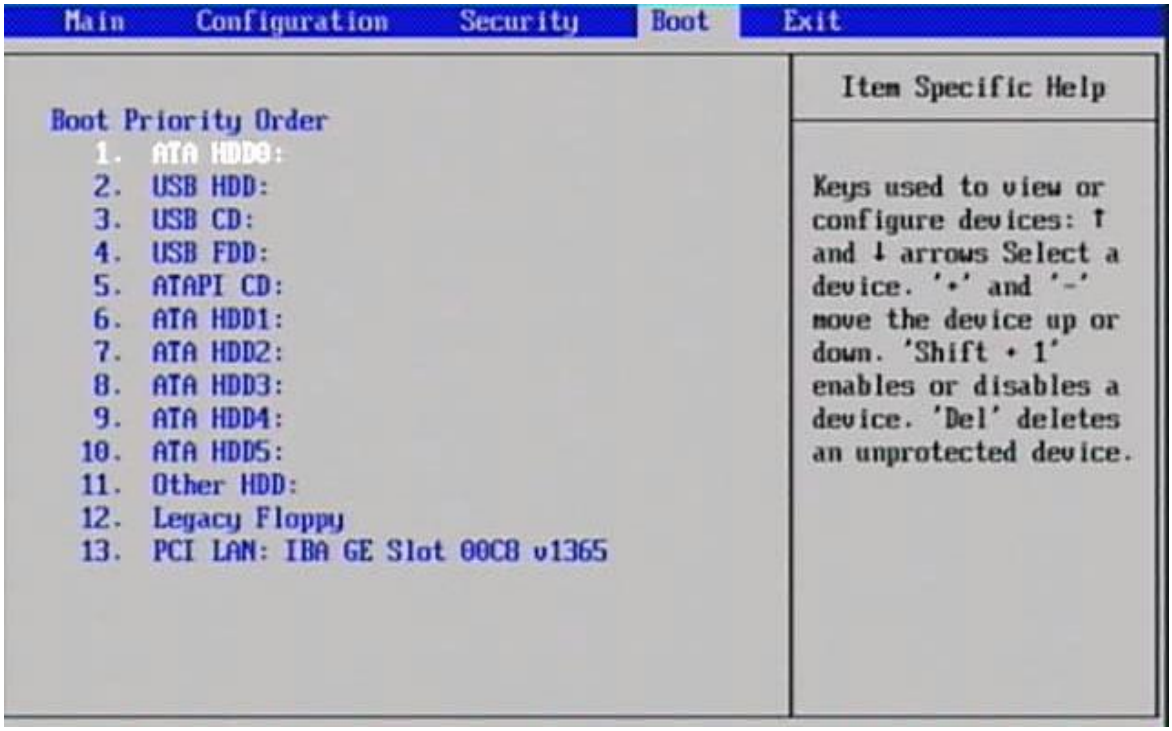
4.4 Chipset

Set or clear the Supervisor account's password.


Phoenix SecureCore Tiano Setup
Main Configuration Security Boot Exit
Supervisor Password is: Cleared
User Password is: Cleared
Set Supervisor Password [Enter]
Supervisor Hint String [ ]
Set User Password [Enter]
User Hint String [ ]
Min. password length [1]
Authenticate User on Boot [Disabled]
HDD Security Status
No HDD detected
Trusted Platform Module (TPM)
Item Specific Help
Set or clear the Supervisor account's password.
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit

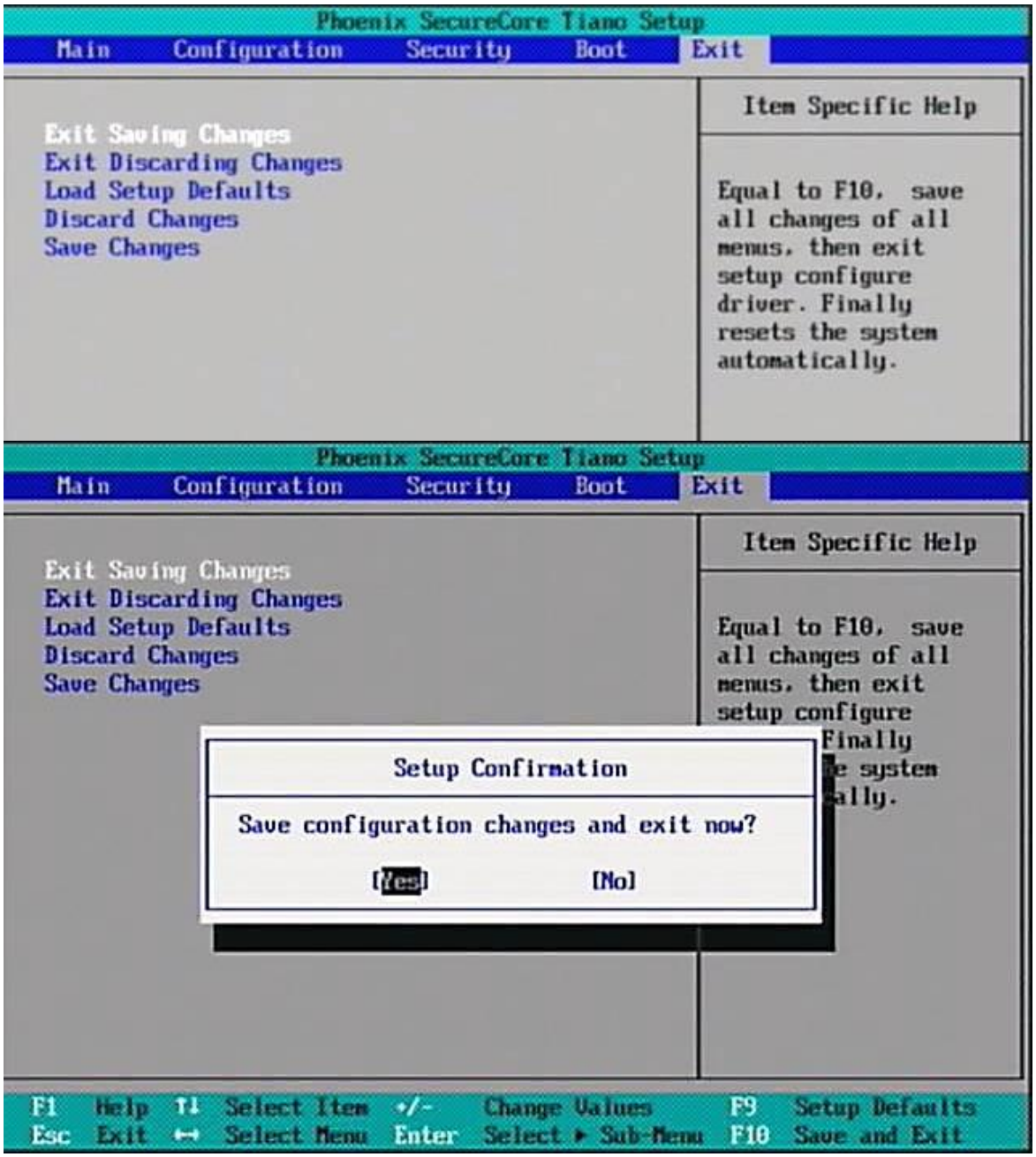
4.5 Boot

Boot Priority Order: Please adjust the order depend of your needs.


Main Configuration Security Boot Exit
Boot Priority Order
1. ATA HDD0:
2. USB HDD:
3. USB CD:
4. USB FDD:
5. ATAPI CD:
6. ATA HDD1:
7. ATA HDD2:
8. ATA HDD3:
9. ATA HDD4:
10. ATA HDD5:
11. Other HDD:
12. Legacy Floppy
13. PCI LAN: IBA GE Slot 00C8 v1365
Item Specific Help
Keys used to view or configure devices: ↑ and ↓ arrows Select a device. '+' and '-' move the device up or down. 'Shift + 1' enables or disables a device. 'Del' deletes an unprotected device.

4.6 Security

Equal to F10, save all changes of all menu, then exit setup configure driver. Finally resets the system automatically.


Phoenix SecureCore Tiano Setup
Main Configuration Security Boot Exit
Exit Saving Changes
Exit Discarding Changes
Load Setup Defaults
Discard Changes
Save Changes
Item Specific Help
Equal to F10, save all changes of all menus, then exit setup configure driver. Finally resets the system automatically.
Setup Confirmation
Save configuration changes and exit now?
[Yes] [No]
F1 Help ↑↓ Select Item +/- Change Values F9 Setup Defaults
Esc Exit ↔ Select Menu Enter Select ▸ Sub-Menu F10 Save and Exit

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get SPI-C2160-LLVA running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting

Unlike other Single board computer, SPI-C2160-LLVA supports ATX only. Therefore, there is no other setting that really needs to be set up. However, there are only two connectors that must be connected—J10 (4 pins CPU +12V main power connector) & 24 pins ATX Power Connector.

Serial ATA Hard Disk Setting for IDE/AHCI

Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total six connectors, J19 & J20, J22, J23 Four ports on-board (those 4 Masters in Non-AHCI mode), two support 6Gb + two support 3Gb and two ports route to backplane support 3Gb, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE and AHCI application for system, please follow up setting guide in BIOS programming (Table 5-1); Furthermore, you can consult chapter 4.3
Advanced "SATA Configuration" part of the" SATA Mode".

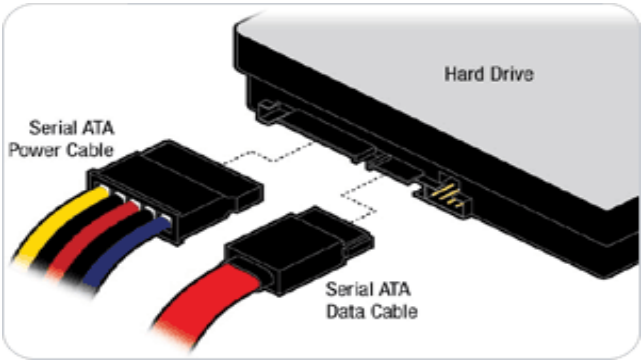


Table. 5-1 SATA Mode setting guide

System BIOS Main Menu

Advanced

SATA Configuration …… [Press enter]

SATA Mode…… [IDE Mode/AHCI Mode]

5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. 240-pin DDR3 Memory, keyboard, mouse, SATA hard disk, VGA connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with SPI-C2160-LLVA, it is recommended, when going with the boot-up sequence, to hit "F2" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting
When prompted with the main setup menu, please scroll down to "Restore Defaults", press "Enter" and select "Yes" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that CONTEC has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Improper Disable Operation
There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the Serial Port1/ Serial Port 2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable Serial Port1 to release IRQ #4
Disable Serial Port2 to release IRQ #3
Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	**System Timer**
IRQ #1	**Keyboard Event**
IRQ #2	**Usable IRQ**
IRQ #3	**COM2**
IRQ #4	**COM1**
IRQ #5	**Usable IRQ**
IRQ #6	**Diskette Event**
IRQ #7	**Usable IRQ**
IRQ #8	**Real-Time Clock**
IRQ #9	**Usable IRQ**
IRQ #10	**Usable IRQ**
IRQ #11	**Usable IRQ**
IRQ #12	**IBM Mouse Event**
IRQ #13	**Coprocessor Error**
IRQ #14	**Hard Disk Event**
IRQ #15	**Usable IRQ**

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Symptom: SBC keeps beeping, and no screen has shown.

Solution: In fact, each beep sound represents different definition of error message. Please refer to table as following:

Beep sounds	Meaning	Action
One long beep with one short beeps	DRAM error	Change DRAM or reinstall it
One long beep constantly	DRAM error	Change DRAM or reinstall it
One long beep with two short beeps	Monitor or Display Card error	Please check Monitor connector whether it inserts properly
Beep rapidly	Power error warning	Please check Power mode setting

Information & Support

Question: I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 2-3 pins on JP9 to clean your password.

Question: How to update the BIOS file of the SPI-C2160-LLVA?

Answer: 1. Please visit web site of the CONTEC download center as below hyperlink and register an account.
http://www.CONTEC.com.tw

2. Input your User name and password to log in the download center.

3. Select the "Search download" to input the keyword "SPI-C2160-LLVA".

4. Find the "BIOS "page to download the ROM file and flash utility.

5. Execute the zip file to root of the bootable USB pen drive.

6. Insert your bootable USB pen drive in SPI-C2160-LLVA board and power-on.

7. Input the "AFUDOS XXXXX.ROM -p -b -n" to start to update BIOS. ("XXXXX" is the file name of the ROM file.)

8. Switch "Off" the Power Supply when you finished the update process.

9. To short the JP9 jumper from 1-2 short to 2-3 short 5 seconds then set back to 1-2 short. (Clear CMOS)

10. Switch "ON" the Power Supply then press the "del" key to BIOS to load "Restore Defaults" and then select "Save Changes and Exit" option.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used for your reference.

Memory Area	Size	Description
0000-003F	1K	Interrupt Area
0040-004F	0.3K	BIOS Data Area
0050-006F	0.5K	System Data
0070-0E2E	54K	DOS
0E2F-0F6B	5K	Program Area
0F6C-9BFF	562K	【Available】
First Meg	-- Conventional memory end at 624K --	
9C00-9D3F	5K	Extended BIOS Area
9D40-9FFF	11K	Unused
A000-AFFF	64K	VGA Graphics
B000-B7FF	32K	Unused
B800-BFFF	32K	VGA Text
C000-CD7F	54K	Video ROM
CD80-EFFF	138K	Unused
F000-FFFF	64K	System ROM
HMA	64K	First 64K Extended

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Interrupt Request Lines IRQ		
IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	【Unassigned】	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ

IRQ 11	**Video ROM**	**Usable IRQ**
IRQ 12	**System ROM**	**IBM Mouse Event**
IRQ 13	**System ROM**	**Coprocessor Error**
IRQ 14	**System ROM**	**Hard Disk Event**
IRQ 15	**【Unassigned】**	**Usable IRQ**